Service Manual

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4. Critical Commpoents List
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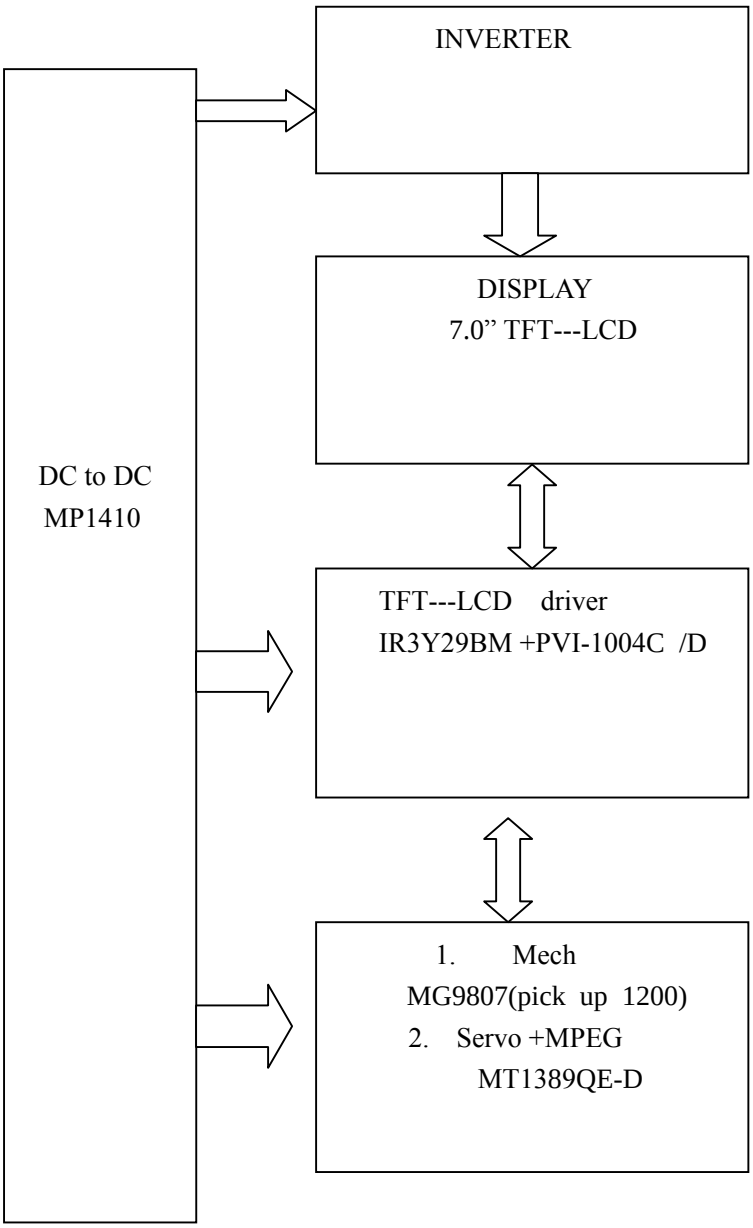
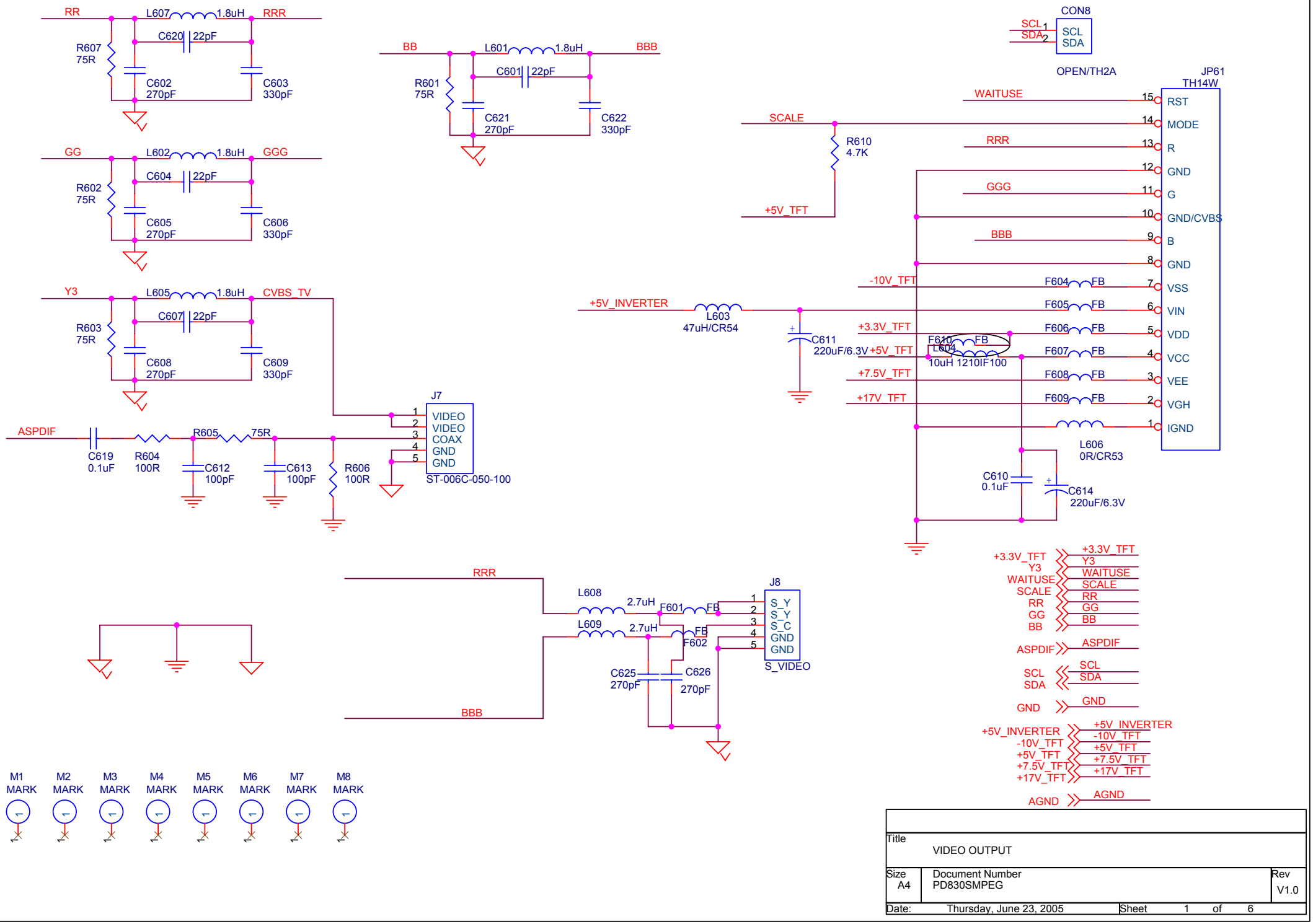
1. The System Block Diagram & the Block's Function Description

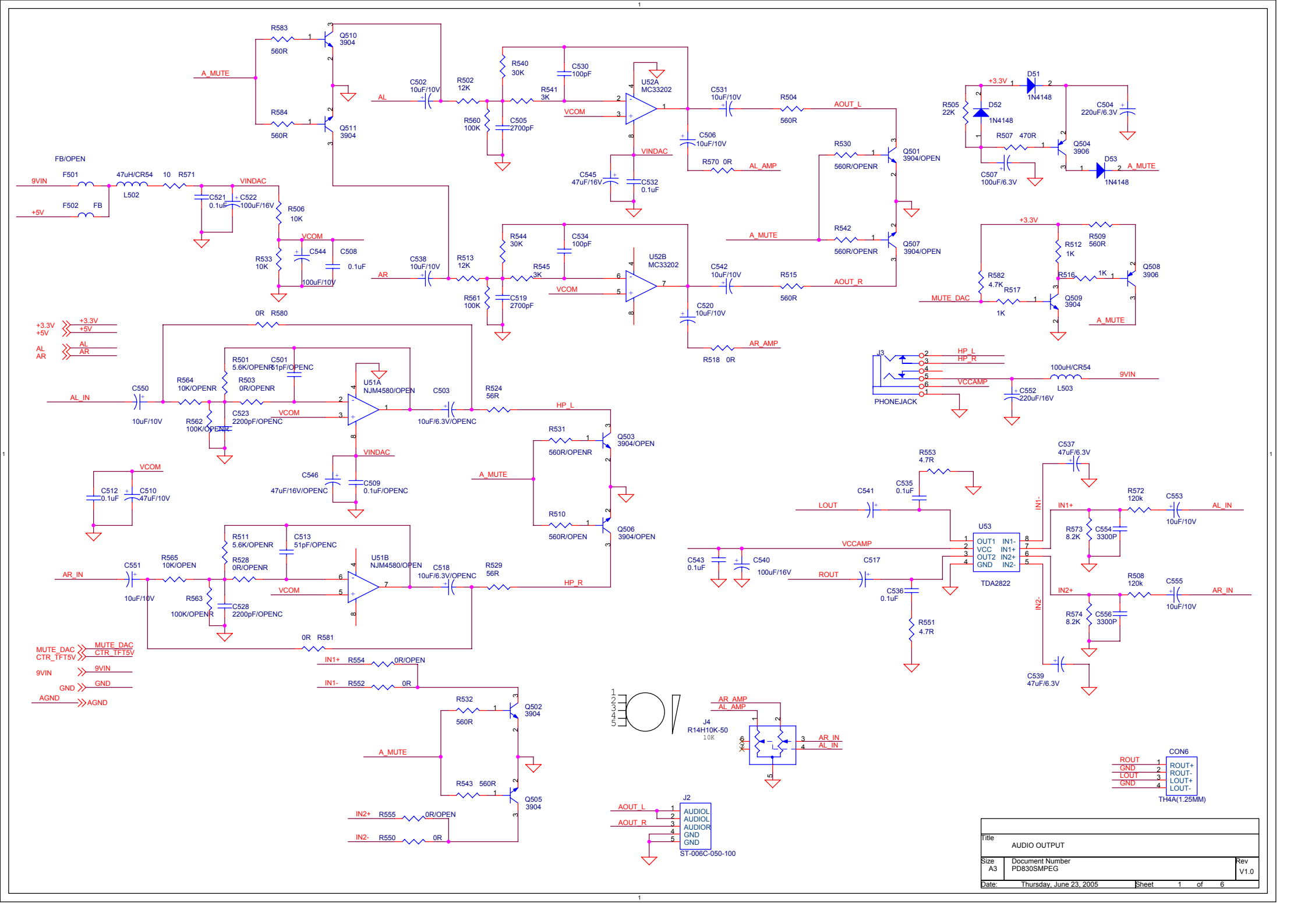
MVDP1075 DVD System Block



2. Schematic Circuit Diagram



Title	VIDEO OUTPUT	
Size A4	Document Number PD830SMPEG	Rev V1.0
Date: Thursday, June 23, 2005	Sheet 1 of 6	



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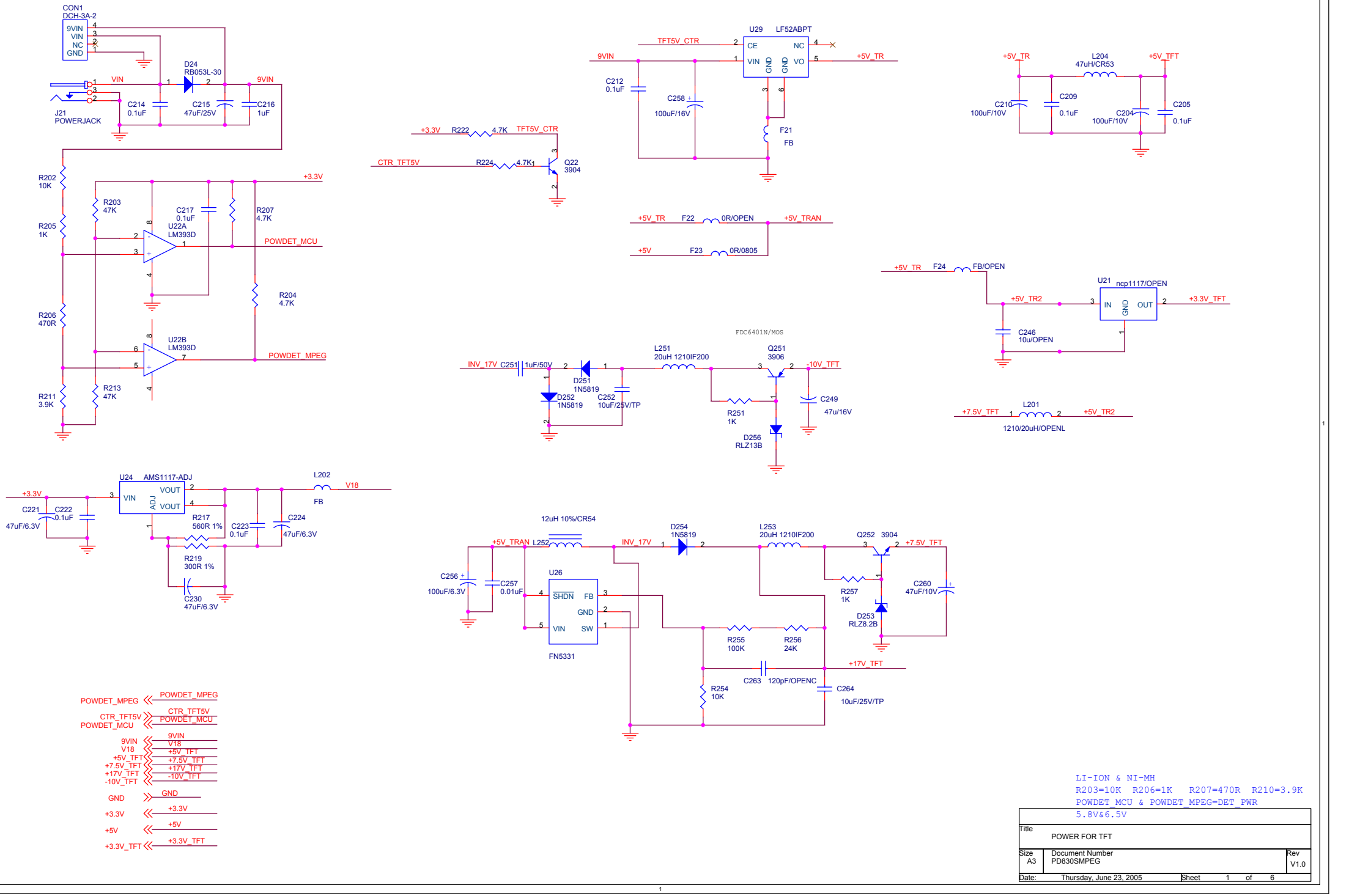
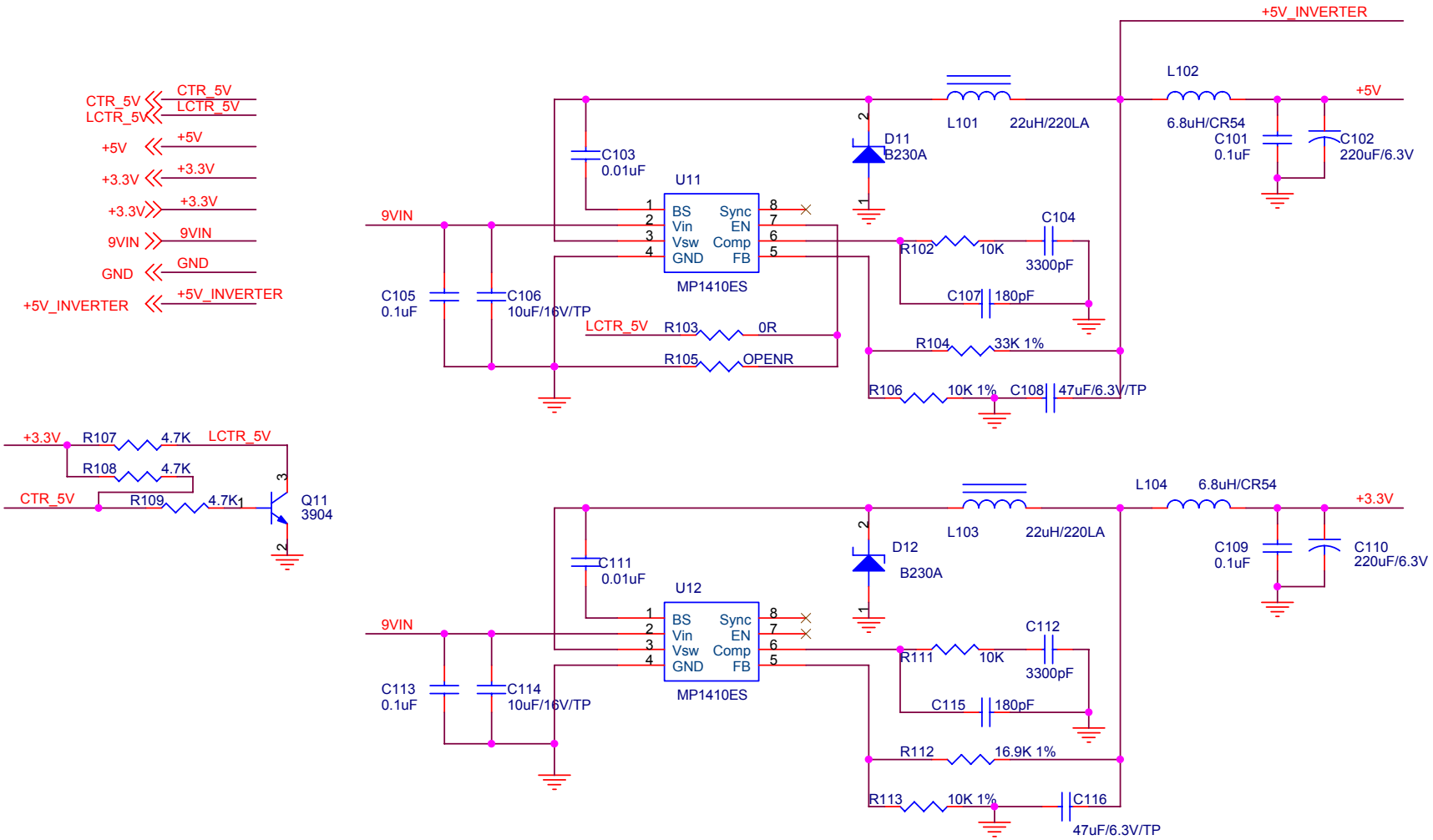
Size A3	Document Number PD830SMPEG	Rev V1.0
Date: Thursday, June 23, 2005	Sheet 1 of 6	

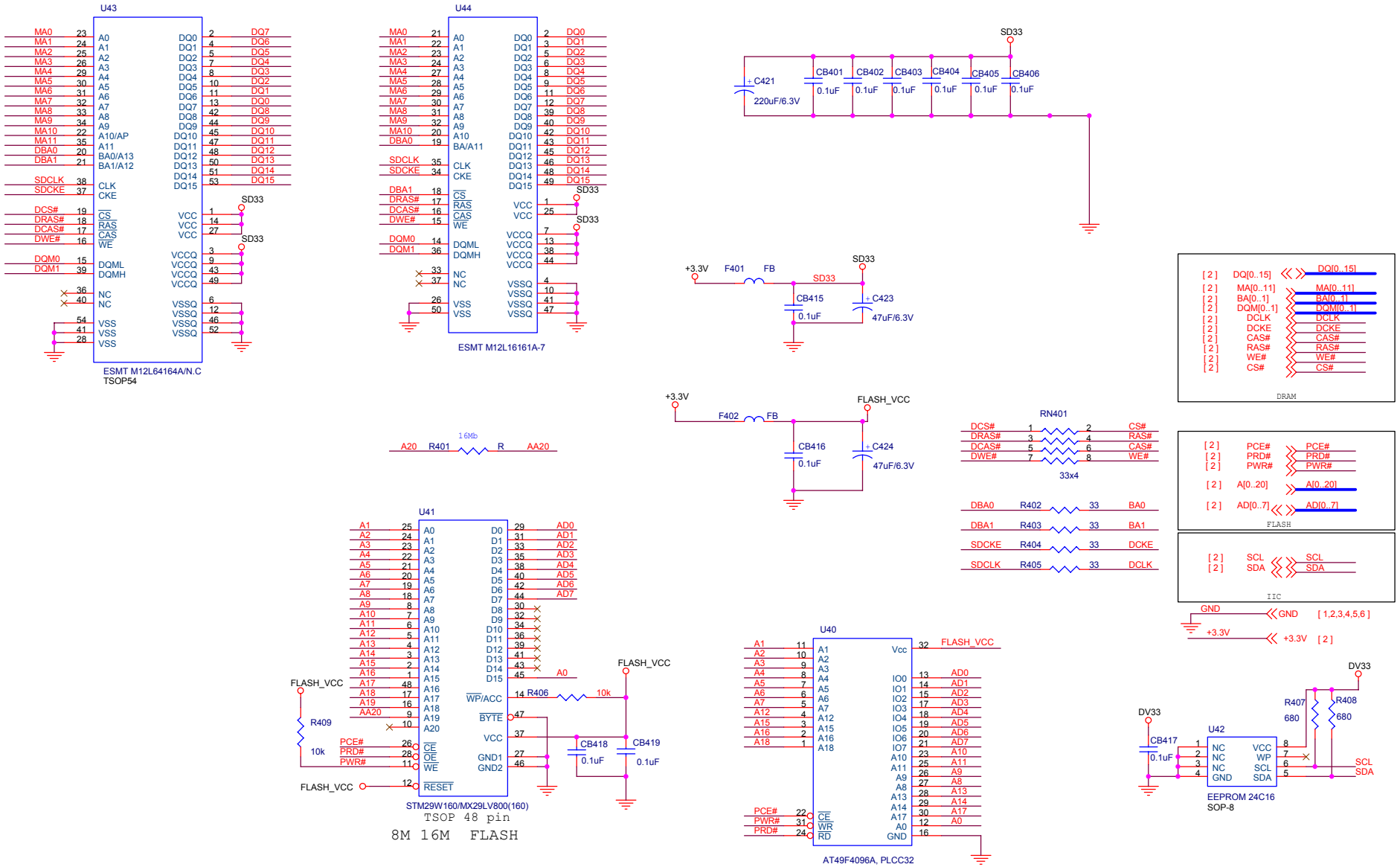


LI-ION & NI-MH
R203=10K R206=1K R207=470R R210=3.9K
POWDET_MCU & POWDET_MPEG=DET_PWR
5.8V&6.5V

Title	POWER FOR TFT	
Size A3	Document Number PD830SMPEG	Rev V1.0
Date: Thursday, June 23, 2005	Sheet 1 of 6	



Title	POWER_CONNECTOR	
Size A4	Document Number PD830SMPEG	Rev V1.0
Date: Thursday, June 23, 2005	Sheet 1 of 6	


U43
ESMT M12L64164A/N.C
TSOP54
U44
ESMT M12L16161A-7
SD33
C421
220uF/6.3V
CB401
CB402
CB403
CB404
CB405
CB406
0.1uF
+3.3V
F401
FB
CB415
C423
47uF/6.3V
DRAM
FLASH_VCC
F402
CB416
C424
RN401
33x4
A20
R401
16Mb
R
AA20
U41
STM29W160/MX29LV800(160)
TSOP 48 pin
8M 16M FLASH
R406
10k
R409
CB418
CB419
U40
AT49F4096A, PLCC32
FLASH
IIC
GND
+3.3V
DV33
U42
EEPROM 24C16
SOP-8
R407
R408
680
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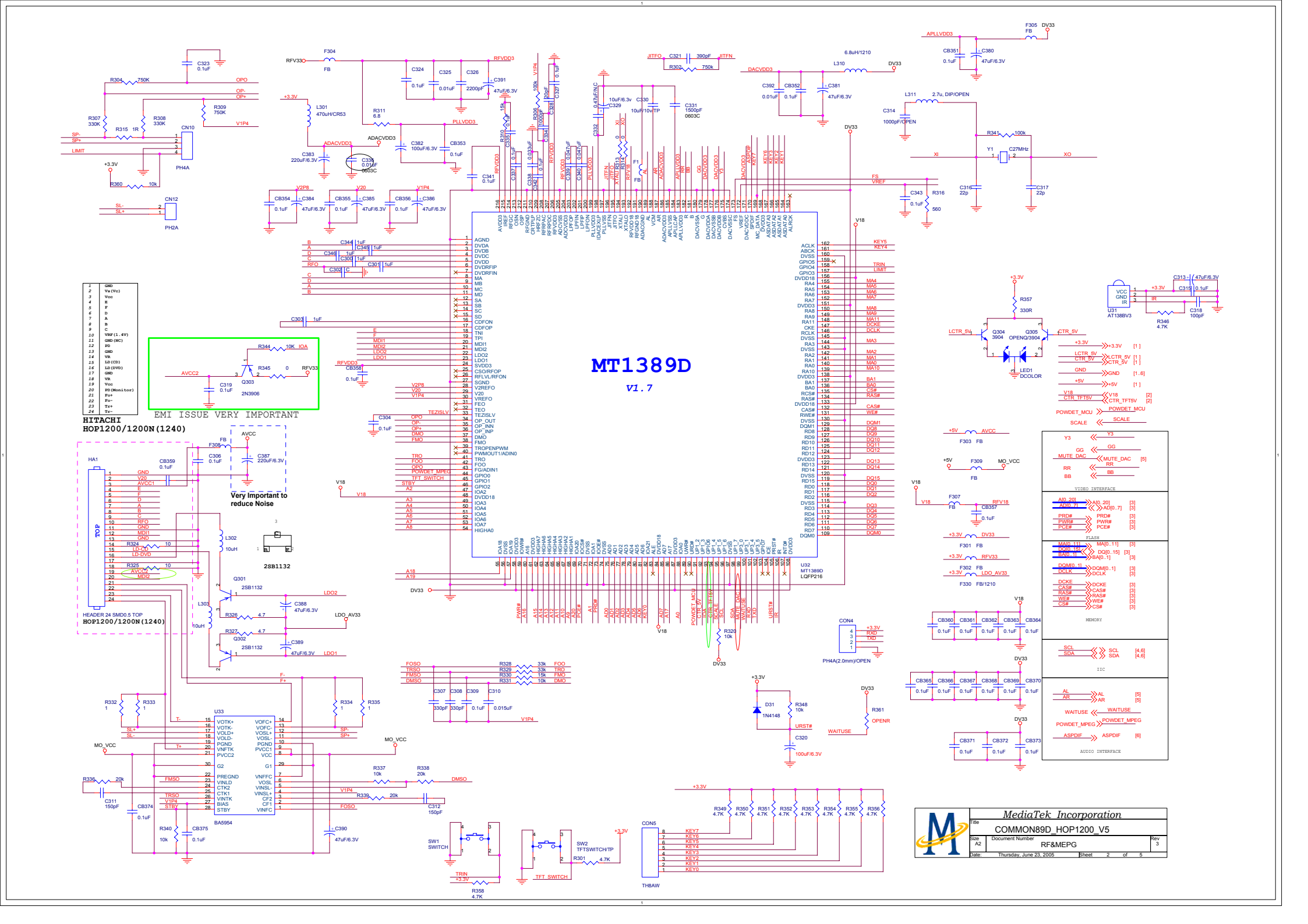
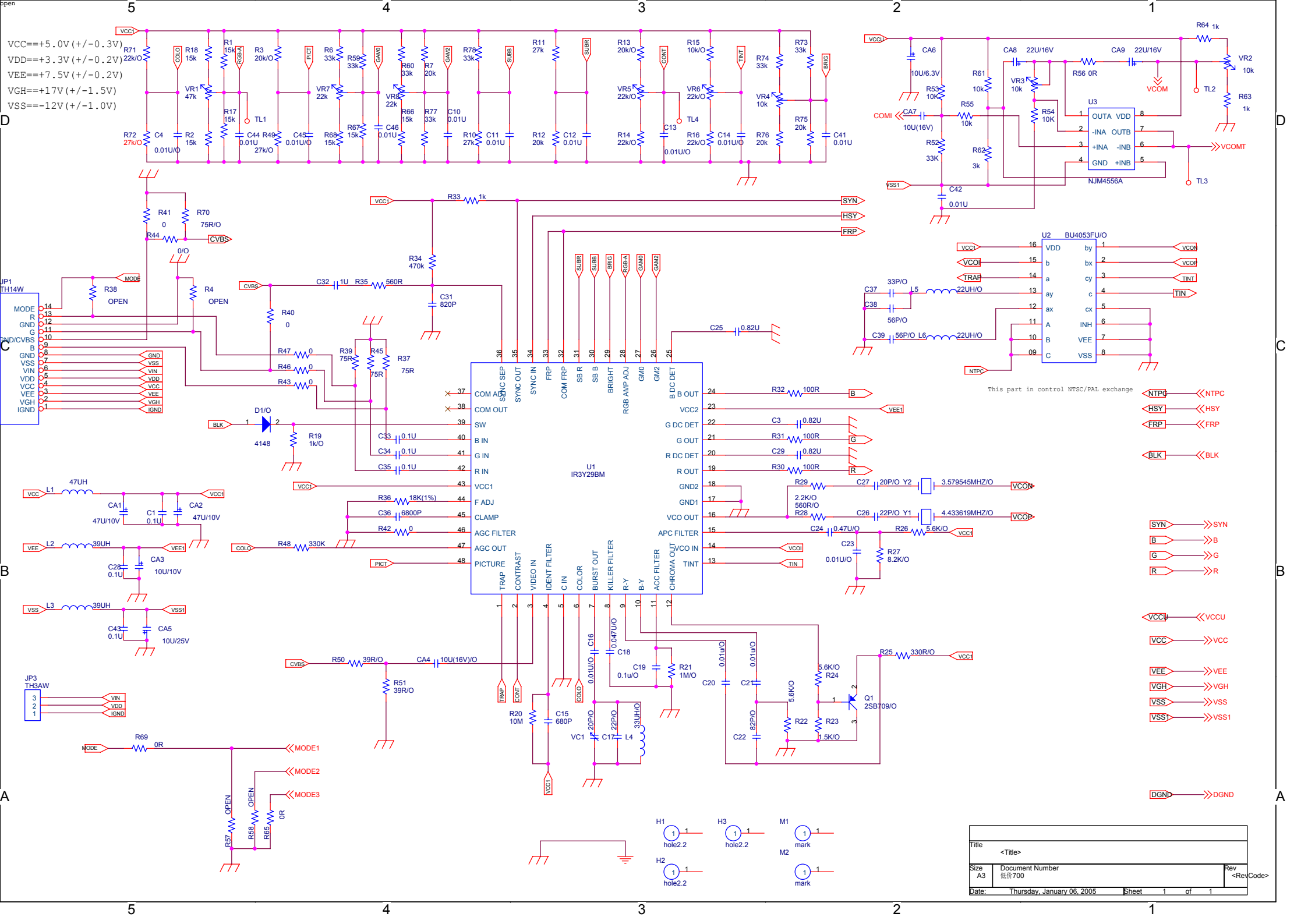

MT1389D
V1.7
HITACHI
HOP1200/1200N(1240)
EMI ISSUE VERY IMPORTANT
Very Important to reduce Noise
HEADER 24 SMD0.5 TOP
HOP1200/1200N(1240)
2SB1132
BA5954
TH8AW
PH4A(2.0mm)/OPEN
MediaTek Incorporation
COMMON89D_HOP1200_V5
RF&MEPG
Thursday, June 23, 2005
VIDEO INTERFACE
FLASH
MEMORY
IIC
AUDIO INTERFACE


VCC==+5.0V(+/-0.3V)
VDD==+3.3V(+/-0.2V)
VEE==+7.5V(+/-0.2V)
VGH==+17V(+/-1.5V)
VSS==-12V(+/-1.0V)
U1
IR3Y29BM
U2
BU4053FU/O
U3
NJM4556A
JP1
TH14W
JP3
TH3AW
Q1
2SB709/O
D1/O
4148
This part in control NTSC/PAL exchange
Title
<Title>
Size
A3
Document Number
低价700
Rev
<RevCode>
Date:
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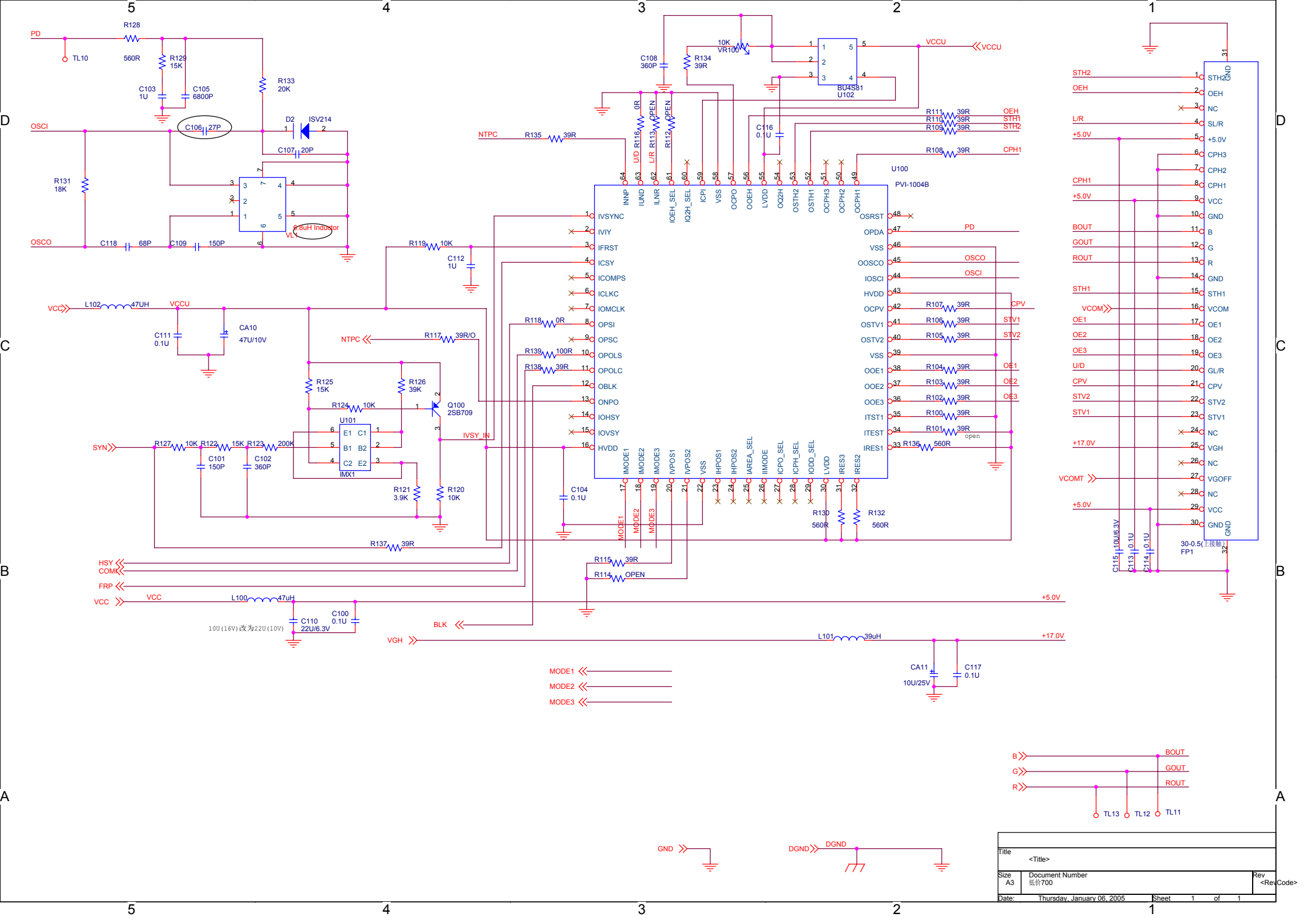
PD
TL10
R128
560R
R129
15K
C103
1U
C105
6800P
R133
20K
OSCI
C106
27P
D2
ISV214
C107
20P
R131
18K
OSCO
C118
68P
C109
150P
VL1
2.8uH Indudtor
U100
PVI-1004B
NTPC
R135
39R
C108
360P
R134
39R
10K
VR100
U102
BU4S31
VCCU
R111
R110
R109
R108
OEH
STH1
STH2
CPH1
C116
0.1U
R119
10K
C112
1U
VCC
L102
47UH
C111
0.1U
CA10
47U/10V
R118
0R
R117
39R/O
R139
100R
R138
39R
R125
15K
R126
39K
R124
10K
Q100
2SB709
U101
IMX1
IVSY_IN
SYN
R127
10K
R122
15K
R123
200K
C101
150P
C102
360P
R121
3.9K
R120
10K
C104
0.1U
R130
560R
R132
560R
R136
560R
R137
39R
R115
39R
R114
OPEN
HSY
COM
FRP
VCC
L100
47uH
C110
22U/6.3V
C100
0.1U
10U(16V)改为22U(10V)
BLK
VGH
L101
39uH
CA11
10U/25V
C117
0.1U
+5.0V
+17.0V
MODE1
MODE2
MODE3
R107
R106
R105
R104
R103
R102
R100
R101
CPV
STV1
STV2
OE1
OE2
OE3
PD
OSCO
OSCI
open
STH2
OEH
L/R
+5.0V
CPH1
BOUT
GOUT
ROUT
VCOM
VCOMT
C115
10U/6.3V
C113
0.1U
C114
0.1U
FP1
30-0.5(上接触)
B
G
R
TL13
TL12
TL11
GND
DGND
Title
<Title>
Size
A3
Document Number
低价700
Rev
<RevCode>
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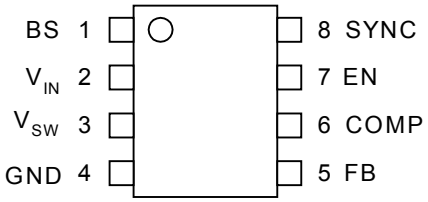
4.Critical Components List

Singing	Appellation
MPS1410	IC
MX29LV800	IC
TDA2822	IC
MT1389D	IC
FN5331	IC
AT5654	IC
MC33202	IC
IR3Y29BM	IC
PVI-1004B	IC

5. IC Date Sheet & IC Description



Pin Functions

BS (Pin 1) Bootstrap

This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between V_{SW} and Bootstrap pins to effect a floating supply across the power switch driver. The voltage across C_B is about 5V and is supplied by the internal +5V supply when the V_{SW} pin voltage is low.

V_{IN} (Pin 2) Supply Voltage

The MP1580 operates from a +4.75 to +25V unregulated input. C_{IN} is needed to prevent large voltage spikes from appearing at the input.

V_{SW} (Pin 3) Switch

This connects the inductor to either the V_{IN} through M1 or to GND through M2.

GND (Pin 4) Ground

This pin is the voltage reference for the regulated voltage. For this reason care must be taken in its layout. This node should be placed outside of the D_{SCH} to C_{IN} ground path to prevent switching current spikes to induce voltage noise into the part.

FB (Pin 5) Feedback

An external resistor divider from the output voltage to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillation frequency when the FB voltage is below 650mV.

COMP (Pin 6) Compensation

This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details.

EN (Pin 7) Enable/UVLO

A voltage greater than 2.495V enables operation. Leave the input unconnected if unused. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from Vin to GND. For complete low current shutdown its needs to be less than 0.7V.

SYNC (Pin 8) Synchronization Input

This pin is used to synchronize the internal oscillator frequency to an external source. There is an internal 11kohm pull down resistor to GND hence leave the input unconnected if unused.

Sync Pin Operation.

The Sync pin driving waveform should be a square wave with a rise time of less than 20ns. Minimum Hi voltage level is 2.7V. Low level is less than 0.8V. The frequency of the external Sync signal needs to be greater than 445 kHz.

A rising edge on the Sync pin forces a reset of the oscillator. The the upper DMOS is switched off immediately if it is not already off. 250nS later the upper DMOS turns on connecting Vsw to Vcc.

Abbr. :

SR : Slew Rate

PU : Pull Up

PD : Pull Down

SMT : Schmitt Trigger

4MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (26)				
191	RFGND18		Ground	Analog ground
192	RFVDD18		Power	Analog power 1.8V
212	OSP		Analog output	RF Offset cancellation capacitor connecting
213	OSN		Analog output	RF Offset cancellation capacitor connecting
214	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
215	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
216	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input
ALPC (4)				

Pin	Main	Alt.	Type	Description
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
26	RFLVL	RFON	Analog output	1) RFRP low pass, or 2) Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (8)				
204	ADCVDD3		Power	Analog 3.3V Power for ADC
205	ADCVSS		Ground	Analog ground for ADC
206	RFVDD3		Power	Analog Power
207	RFRPDC		Analog output	RF ripple detect output
208	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
209	HRFZC		Analog Input	High frequency RF ripple zero crossing
210	CRTPLP		Analog output	Defect level filter capacitor connecting
211	RFGND		Ground	Analog Power
RF Data PLL Interface (9)				
195	JITFO		Analog output	The output terminal of RF jitter meter.
196	JITFN		Analog Input	The input terminal of RF jitter meter.
197	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.
198	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
199	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
200	LPFON		Analog Output	The negative output of loop filter amplifier
201	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
202	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
203	LPFOP		Analog Output	The positive output of loop filter amplifier

Pin	Main	Alt.	Type	Description
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENPWM		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT1	ADIN0	Analog Output	1) 1st General PWM output, or 2) AD input 0
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
43	FG (Diogital pin)	ADIN1 GPIO	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for ADIN1	1) Motor Hall sensor input, or 2) AD input 1, or 3) GPIO
General Power/Ground (27)				
48,84, 133,156	DVDD18		Power	1.8V power pin for internal digital circuitry
71,120, 143	DVSS		Ground	1.8V Ground pin for internal digital circuitry
58,61,87, 108,123,138, 151,168	DVDD3		Power	3.3V power pin for internal digital circuitry
56,74,97, 115,130,145, 160	DVSS		Ground	3.3V Ground pin for internal digital circuitry
184	APLLCAP		Analog Inout	APLL External Capacitance connection
185	APLLVSS		Ground	Ground pin for audio clock circuitry
183	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
Micro Controller and Flash Interface (48)				
54	HIGHA0		Inout 4~16MA, SR PU	Microcontroller address 8
68	HIGHA1		Inout 4~16MA, SR PU	Microcontroller address 9
67	HIGHA2		Inout 4~16MA, SR PU	Microcontroller address 10

Pin	Main	Alt.	Type	Description
66	HIGHA3		Inout 4~16MA, SR PU	Microcontroller address 11
65	HIGHA4		Inout 4~16MA, SR PU	Microcontroller address 12
64	HIGHA5		Inout 4~16MA, SR PU	Microcontroller address 13
63	HIGHA6		Inout 4~16MA, SR PU	Microcontroller address 14
62	HIGHA7		Inout 4~16MA, SR PU	Microcontroller address 15
85	AD7		Inout 4~16MA, SR	Microcontroller address/data 7
81	AD6		Inout 4~16MA, SR	Microcontroller address/data 6
80	AD5		Inout 4~16MA, SR	Microcontroller address/data 5
79	AD4		Inout 4~16MA, SR	Microcontroller address/data 4
78	AD3		Inout 4~16MA, SR	Microcontroller address/data 3
77	AD2		Inout 4~16MA, SR	Microcontroller address/data 2
76	AD1		Inout 4~16MA, SR	Microcontroller address/data 1
75	AD0		Inout 4~16MA, SR	Microcontroller address/data 0
88	IOA0		Inout 4~16MA, SR PU	Microcontroller address 0 / IO
72	IOA1		Inout 4~16MA, SR PU	Microcontroller address 1 / IO
47	IOA2		Inout 4~16MA, SR PU	Microcontroller address 2 / IO
49	IOA3		Inout 4~16MA, SR PU	Microcontroller address 3 / IO
50	IOA4		Inout 4~16MA, SR PU	Microcontroller address 4 / IO

Pin	Main	Alt.	Type	Description
51	IOA5		Inout 4~16MA, SR PU	Microcontroller address 5 / IO
52	IOA6		Inout 4~16MA, SR PU	Microcontroller address 6 / IO
53	IOA7		Inout 4~16MA, SR PU	Microcontroller address 7 / IO
60	A16		Output 4~16MA, SR PU	Flash address 16
86	A17		Output 4~16MA, SR PU	Flash address 17
55	IOA18		Inout 4~16MA, SR PD, SMT	Flash address 18 / IO
57	IOA19		Inout 4~16MA, SR PD, SMT	Flash address 19 / IO
69	IOA20		Inout 4~16MA, SR PD, SMT	Flash address 20 / IO
82	IOA21	GPIO	Inout 4~16MA, SR PD, SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: GPIO
83	ALE		Inout 4~16MA, SR PU, SMT	Microcontroller address latch enable
73	IOOE#		Inout 4~16MA, SR SMT	Flash output enable, active low / IO
59	IOWR#		Inout 4~16MA, SR PU, SMT	Flash write enable, active low / IO
70	IOCS#		Inout 4~16MA, SR SMT	Flash chip select, active low / IO
89	UWR#		Inout 4~16MA, SR PU, SMT	Microcontroller write strobe, active low
90	URD#		Inout 4~16MA, SR PU, SMT	Microcontroller read strobe, active low

Pin	Main	Alt.	Type	Description
91	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
92	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
94	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
95	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
96	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
98	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
99	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
100	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
101	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin
102	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
106	IR		Input SMT	IR control signal input
107	INT0#		Inout 4~16MA, SR PU, SMT	Microcontroller external interrupt 0, active low
Audio interface (14)				
163	ALRCK	GPO	Inout 4MA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I) 1 : use external 373 II) 0: use internal 373 3) While internal AUDIO DAC used: GPO
161	ABCK	GPIO	Inout 4MA	1) Audio bit clock 2) While internal AUDIO DAC used: GPIO

Pin	Main	Alt.	Type	Description
162	ACLK	GPIO	Inout 4MA SMT	1) Audio DAC master clock 2) While internal AUDIO DAC used: GPIO
164	ASDATA0	GPO	Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While internal AUDIO DAC used: GPO
165	ASDATA1	GPO	Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While only 2 channels output: GPO
166	ASDATA2	GPO	Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While only 2 channels output: GPO
167	ASDATA3	GPIO	Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) While only 2 channels output: GPIO
169	MC_DATA	INT2# GPIO	Inout 2MA	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPIO
170	SPDIF		Output 4~16MA, SR : ON/OFF	SPDIF output
186	ADACVDD3		Power	3.3V power pin for AUDIO DAC circuitry
187	AR	GPO	Output	1) AUDIO DAC right channel output 2) While internal AUDIO DAC not used: GPO
188	VCM		Analog	AUDIO DAC reference voltage
189	AL	GPO	Output	1) AUDIO DAC left channel output 2) While internal AUDIO DAC not used: GPO
190	ADACGND		Ground	Ground pin for AUDIO DAC circuitry
Video Interface (12)				
171	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
172	VREF		Analog	Bandgap reference voltage
173	FS		Analog	Full scale adjustment
174	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
175	CVBS		Output 4MA, SR	Analog composite output
176	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
177	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
178	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry

Pin	Main	Alt.	Type	Description
179	Y/G		Output 4MA, SR	Green or Y or SY or CVBS
180	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
181	B/CB/PB		Output 4MA, SR	Blue or CB/PB or SC
182	R/CR/PR		Output 4MA, SR	Red or CR/PR or CVBS or SY
MISC (10)				
105	PRST#		Input PU, SMT	Power on reset input, active low
104	ICE		Input PD, SMT	Microcontroller ICE mode enable
193	XTALO		Output	27M crystal out
194	XTALI		Input	27M crystal in
44	GPIO0	VSYN	Inout 4MA, SR SMT	1) General purpose IO 0 2) Vertical sync for video-input
45	GPIO1	HSYN INT4#	Inout 4MA, SR SMT	1) General purpose IO 1 2) Horizontal sync for video-input 3) Microcontroller external interrupt 4
46	GPIO2		Inout 2MA	General purpose IO 2
157	GPIO3	INT1#	Inout 2MA	1) General purpose IO 3 2) Microcontroller external interrupt 1
158	GPIO4		Inout 2MA	General purpose IO 4
159	GPIO5	INT3#	Inout 2MA	1) General purpose IO 5 2) Microcontroller external interrupt 3
93	GPIO6		Inout 4MA, SR PD, SMT	General purpose IO 6
103	GPIO7		Inout 4MA, PD, SMT	General purpose IO 7
Dram Interface (38) (Sorted by position)				
155	RA4		Inout	DRAM address 4
154	RA5		Inout	DRAM address 5
153	RA6		Inout	DRAM address 6
152	RA7		Inout	DRAM address 7
150	RA8		Inout	DRAM address 8
149	RA9		Inout	DRAM address 9
148	RA11		Inout Pull-Down	DRAM address bit 11

Pin	Main	Alt.	Type	Description
147	CKE		output	DRAM clock enable
146	RCLK		Inout	Dram clock
144	RA3		Inout	DRAM address 3
142	RA2		Inout	DRAM address 2
141	RA1		Inout	DRAM address 1
140	RA0		Inout	DRAM address 0
139	RA10		Inout	DRAM address 10
137	BA1		Inout	DRAM bank address 1
136	BA0		Inout	DRAM bank address 0
135	RCS#		output	DRAM chip select, active low
134	RAS#		output	DRAM row address strobe, active low
132	CAS#		output	DRAM column address strobe, active low
131	RWE#		output	DRAM Write enable, active low
129	DQM1		Inout	Data mask 1
128	RD8		Inout	DRAM data 8
127	RD9		Inout	DRAM data 9
126	RD10		Inout	DRAM data 10
125	RD11		Inout	DRAM data 11
124	RD12		Inout	DRAM data 12
122	RD13		Inout	DRAM data 13
121	RD14		Inout	DRAM data 14
119	RD15		Inout	DRAM data 15
118	RD0		Inout	DRAM data 0
117	RD1		Inout	DRAM data 1
116	RD2		Inout	DRAM data 2
114	RD3		Inout	DRAM data 3
113	RD4		Inout	DRAM data 4
112	RD5		Inout	DRAM data 5
111	RD6		Inout	DRAM data 6
110	RD7		Inout	DRAM data 7
109	DQM0		Inout	Data mask 0

Note:

1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The multi-function GPO pins are ser to blue characters.
4. The external TV encoder mode only supports CCIR-656 mode.
5. Compare to MT1389B/MT1389C,
   GPIO0 <--> VSYN
   GPIO1 <--> HSYN
   GPIO2 <--> SPMCLK
   GPIO3 <--> SPDATA
   GPIO4 <--> SPLRCK
   GPIO5 <--> SPBCK
6. bonding option
   pin 93 optional to GPIO6 <--> YUV7

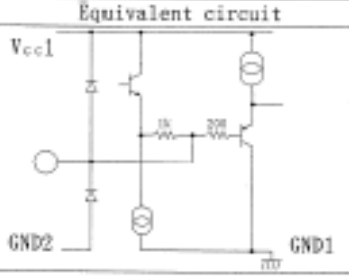
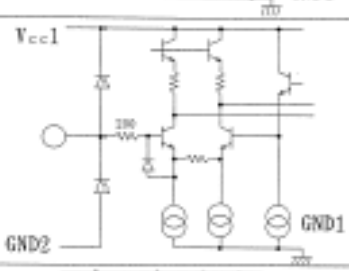
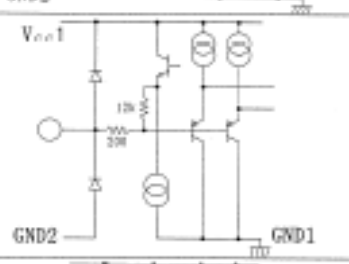
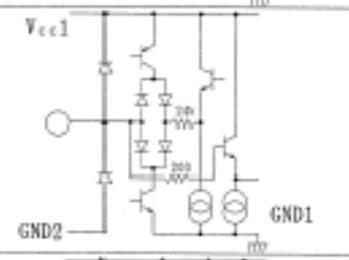
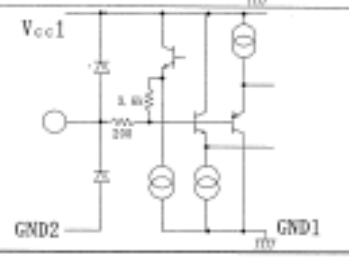
pin 103 optional to GPIO7 <--> ASDATA4

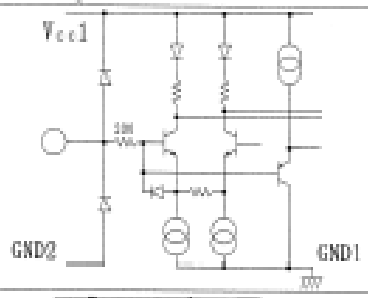
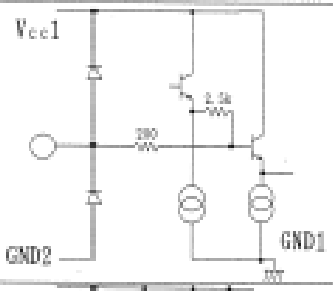
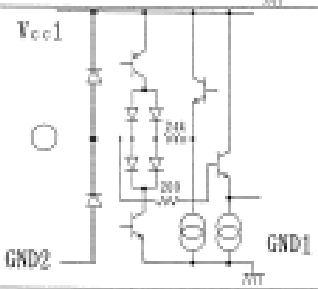
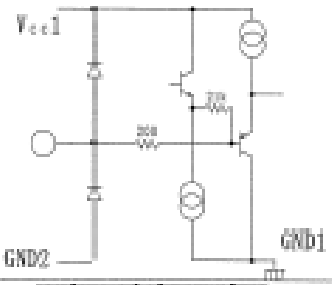
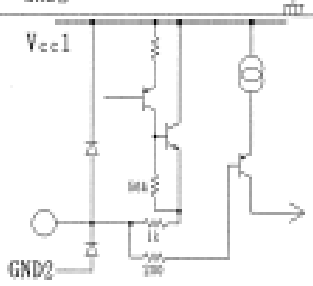
Revision History:

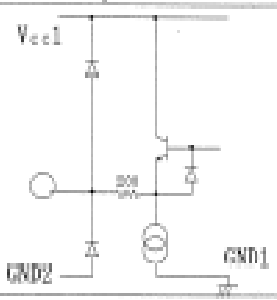
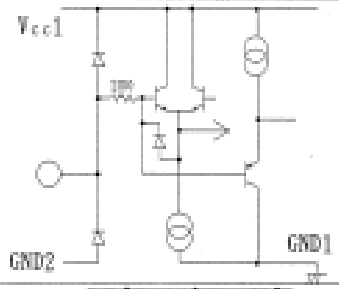
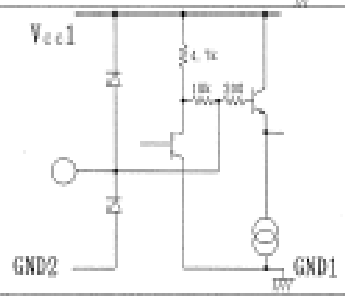
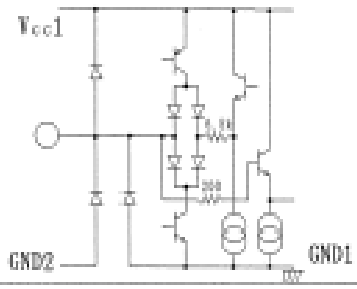
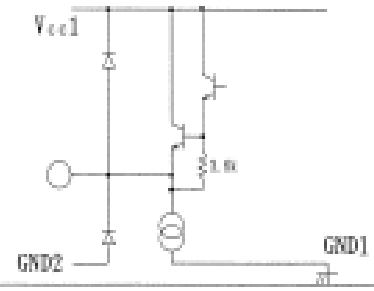
Date	Version	Content
2004-01-10	1.0	● Document Initial
2004-02-10	1.1	● Pin re-define
2004-02-13	1.2	● Pin 86 change to A17, Pin 87 change to DVDD3
2004-02-16	1.3	● Pin 161 change to ABCK, Pin162 change to ACLK, Pin 163 change to ALRCK ● Pin 182 add SY or CVBS output, Pin 180 add SC output, Pin 179 add CVBS or SY output
2004-02-18	1.4	● Reverse video dac pin order (pin179 ~ pin190)
2004-02-19	1.5	● Remove RA11 as GPIO ● Change ACLK, ASDATA0, ASDATA1, ASDATA2 GPIO function to GPO only ● Change video dac, audio dac, apll pin position
2004-03-01	1.6	● Change pin APLLVDD3 to pin 183, pin APLLVSS to pin 185
2004-03-02	1.7	● Change pin 51 ~ pin 63 assignment
2004-05-18	1.8	● Change pin 93 to GPIO6, pin 103 to GPIO7
2004-06-10	1.9	● Pin 44 add alternative function VSYN ● Pin 45 add alternative function HSYN

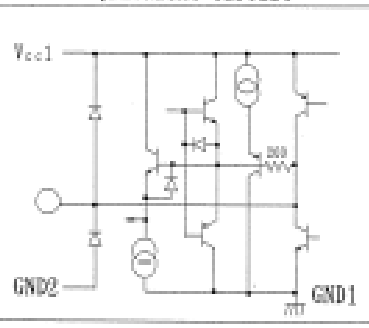
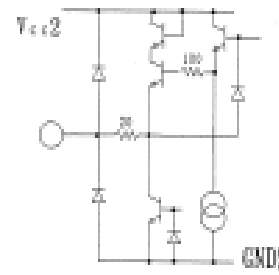
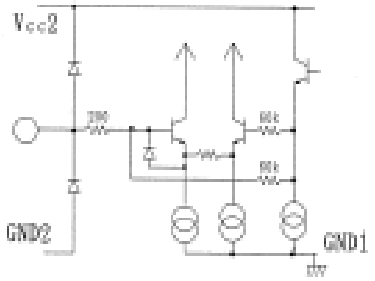
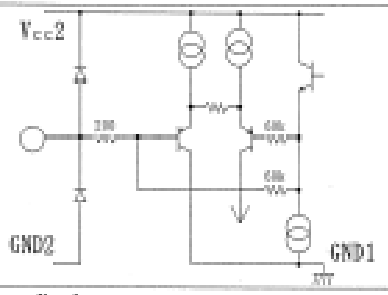
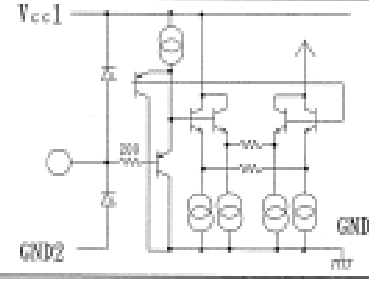
IR3Y29BM Pin Description

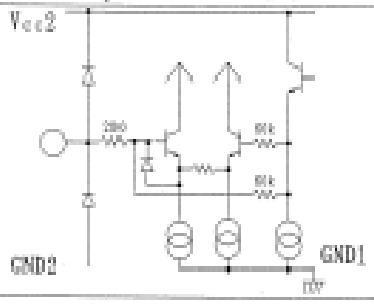
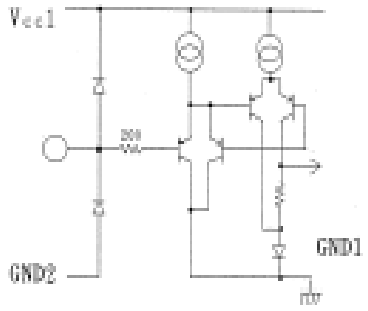
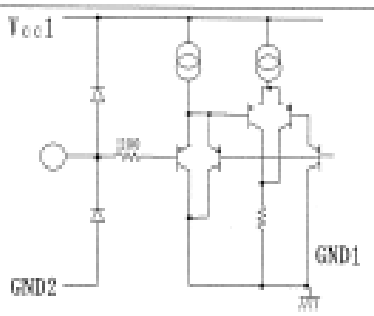
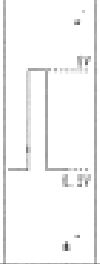
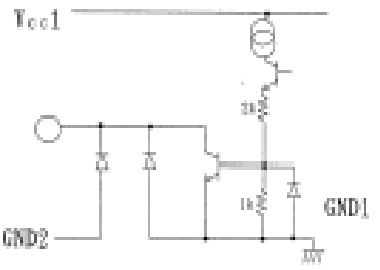
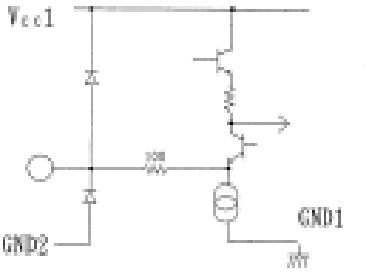
5. Description of Terminals (Vcc1=5.0V/Vcc2=7.5V These voltage are typical value.)

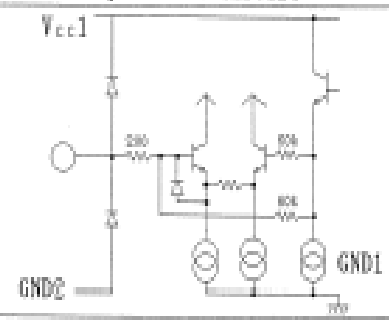
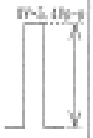
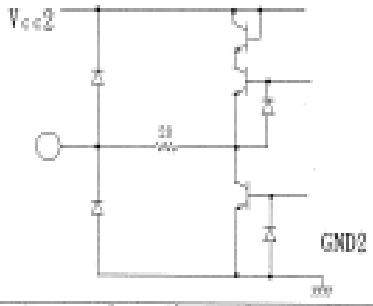
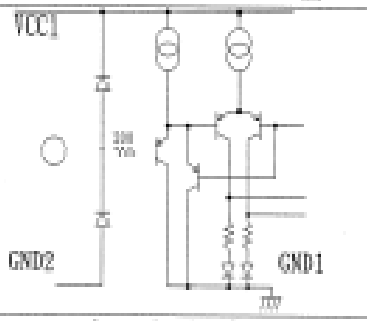
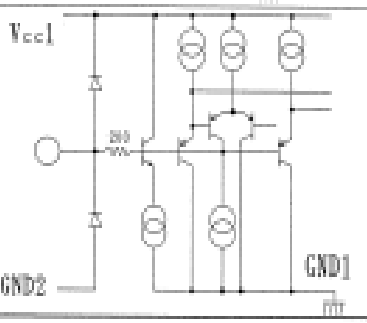
Pin. No.	Term. Name	Voltage	Equivalent circuit	Description
1	TRAP	2.2V		This terminal is connected to the TRAP filter. Output impedance:1kΩ
2	CONTRAST	1.1V ~3.7V		The DC voltage applied to this terminal adjusts the contrast of the composite or Y/C video signal.
3	VIDEO IN	2.2V		Input the composite video signal to this terminal. (In case of using the Y/C video signal, input the luminance signal.)
4	IDENT FILTER	1.0V -		This terminal is connected to the IDENT detection filter.
5	C IN	2.7V		In case of using the Y/C video signal, input the chrominance signal. In case of using the composite video signal, connect this terminal to the ground.

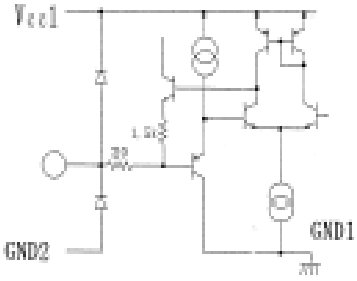
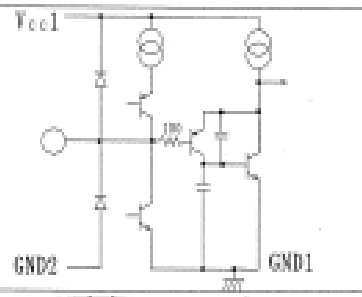
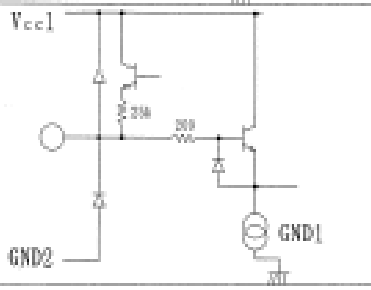
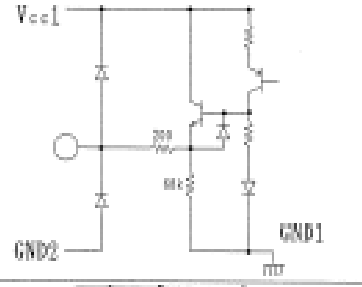
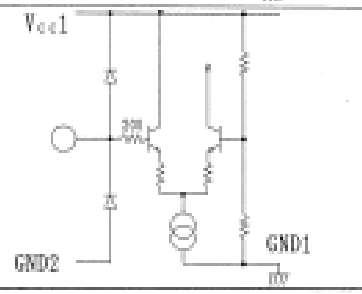
Term. No.	Term. Name	Voltage	Equivalent Circuit	Description
6	COLOR	1.8V ~4.1V		The DC voltage applied to this terminal adjusts the color gain.
7	BURST OUT	3.5V		In case of the PAL mode, this terminal is connected to the burst cleaning coil.
8	KILLER FILTER	1.7V		This terminal is connected to the KILLER detection filter.
9 10	R-Y B-Y	2.2V		Input the chrominance signal for the PAL demodulate circuit.
11	ACC FILTER	1.8V		This terminal is connected to the ACC detection filter.

Term. No.	Term. Name	voltage	Equivalent Circuit	Description
12	CHROMA OUT	2.7V		This terminal outputs the chrominance signal whose color gain has been adjusted and whose burst signal has been removed.
13	TINT	0V ~5V		The voltage applied to this terminal adjusts the tint. This terminal also switches between the NTSC mode and the PAL mode. In case of the PAL mode, connect this terminal to the ground.
14	VCO IN	4.2V		The input terminal of the VCO circuit.
15	APC FILTER	2.6V		This terminal is connected to the APC detection filter.
16	VCO OUT	2.2V		The output terminal of the VCO circuit.
17, 18	GND1, 2	0V		The terminals of GND1 and GND2 are not connected together. Be sure that these terminals should be connected with the same voltage.

Term. No.	Term. Name	Voltage	Equivalent Circuit	Description
20 22 25	R DC DET G DC DET B DC DET	2.3V		This terminal is connected to the capacitor that smooths and holds the DC voltage of the RGB outputs. Because of the high impedance, use low leakage current capacitor.
19 21 24	R OUT G OUT B OUT	$\frac{Vcc1}{2}$ ≒2.5V		Output terminal of the RGB signals.
23	Vcc2			Connect to the power supply for the RGB outputs.
26	GAMMA 2	1.2V ～3.5V		The DC voltage applied to this terminal adjusts the γ2 point. This terminal is pre-set inside the IC.
28	RGB AMPLITUDE ADJUST	1.2V ～3.5V		The DC voltage applied to this terminal adjusts the amplitude (BLK-BLK) of the RGB output signals and the dynamic range. This terminal is preset inside the IC.
27	GAMMA 0	1.2V ～3.5V		The DC voltage applied to this terminal adjusts γ0 point. This terminal is preset inside the IC.
29	BRIGHT	0.7V ～2.6V		The DC voltage applied to this terminal adjusts the position of the gamma correction curve and the amplitude of the common voltage.

Term. No.	Term. Name	voltage	Equivalent Circuit	Description
30 31	SUB BRIGHT B SUB BRIGHT R	1.0V ~3.5V		The DC voltage applied to these terminals adjust the brightness of the R and B signals finely by moving the gamma correction curve. These terminals are preset inside the IC.
32	COMMON FRP			Input the switching signal of the common output.
33	FRP			Input the inverting signal of the RGB outputs. "LOW":Inverting. "HI" :Not inverting.
34	SYNC IN			Input the horizontal synchronizing pulse.(Active Low) In case of the PAL mode, inner flip-flop switches at the rising edge of the input pulse.
35	SYNC OUT			Outputs the composite synchronizing pulse separated by the SYNC-separation circuit. (Active High) The output is provided by an open collector circuit.
36	SYNC SEP	2.0V		The input terminal of the video signal for the SYNC-separation circuit.

Term.No.	Term. Name	Voltage	Equivalent Circuit	Description
37	COMMON AMPLITUDE ADJUST	1.0V ~3.5V		The DC voltage applied to this terminal adjusts the amplitude of the COM output. This terminal is preset inside the IC.
38	COMMON OUT			The output terminal of the COM signal.
39	SW			Input the video source selection signal. Give the "Low" level in case of the composite or Y/C input, and give the "High" level or open in case of the RGB inputs.
40 41 42	B IN G IN R IN	2.2V		The input terminal of the RGB signals. The signal is required to be AC coupled.

Term.No.	Term. Name	Volage	Equivalent Circuit	Description
43	$V_{cc}1$			Connect to the power supply.
44	F ADJ	1.3V		The resistor between this terminal and the ground adjusts the frequency characteristic of the inner filters. The resistor of 18k ohms is recommended for the both mode. Resistance accuracy:±2% Temp. Stability:±200ppm/℃
45	CLAMP	2.4V		Connect the capacitor that clamps the pedestal level of the luminance signal. Because of the high impedance, use the low leackage carrent capacitor.
46	AGC FILTER	2.9V		Connect the AGC detection filter for luminance signal.
47	AGC OUT	0.75V ~3.1V		This terminal outputs the AGC detection voltage of the luminance signal. The output voltage increases with the increase of the AGC gain.
48	PICTURE	1.6V ~3.6V		The DC voltage applied to this terminal adjusts the frequency characteristic of the luminance signal. The outline is emphasized by reducing the voltage of this terminal.

3. Pin assignment

pin No.	pin name	I/O	Remarks	pin No.	pin name	I/O	Remarks
1	ivsync	I	schimtt	33	ires1	I	pull_down
2	iviy	I	schimtt	34	itest	I	pull_up
3	ifrst	I	schimtt	35	itst1	I	AC/DC test
4	icsy	I	schimtt	36	ooe3	O	1mA
5	icomps	I	pull_up	37	ooe2	O	1mA
6	iclkc	I	pull_up	38	ooe1	O	1mA
7	iomclk	I/O	Bi dir.(3mA)	39	VSS		
8	opsi	O	1mA	40	ostv2	O	3_state(1mA)
9	opsc	O	1mA	41	ostv1	O	3_state(1mA)
10	opols	O	3mA	42	ocpv	O	3mA
11	opolc	O	3mA	43	HVDD		5.0V
12	oblk	O	1mA	44	iosci	I	xin (25Mhz)
13	onpo	O	1mA	45	oosco	O	xout(25Mhz)
14	iohsy	I/O	Bi dir.(3mA)	46	VSS		
15	iovsy	I/O	Bi dir(3mA).	47	opda	O	3_state(3mA)
16	HVDD		5.0V	48	osrst	O	1mA
17	imode1	I	pull_down	49	ocph1	O	3mA
18	imode2	I	pull_down	50	ocph2	O	3mA
19	imode3	I	pull_down	51	ocph3	O	3mA
20	ivpos1	I	pull_up	52	osth1	O	3_state(1mA)
21	ivpos2	I	pull_up	53	osth2	O	3_state(1mA)
22	VSS			54	oq2h	O	3mA
23	ihpos1	I	pull_up	55	LVDD		3.3V
24	ihpos2	I	pull_up	56	ooeh	O	3mA
25	iarea_sel	I	pull_up	57	ocpo	O	3mA
26	iimode	I	pull_up	58	VSS		
27	icpo_sel	I	pull_up	59	icpi	I	schmitter
28	icph_sel	I	pull_up	60	iq2h_sel	I	pull_up
29	iodd_sel	I	pull_up	61	ioeh_sel	I	pull_up
30	LVDD		3.3V	62	ilnr	I	pull_up
31	ires3	I	pull_down	63	iund	I	pull_up
32	ires2	I	pull_down	64	innp	I	pull_up

4. Pin Description

No.	Symbol	I/O	Description	Remark
1	ivsync	I	vertical sync signal in composite sync mode (low active)	
2	iviy	I	vertical sync signal in separate sync mode(low active)	
3	ifrst	I	reset pin in ASIC 1) ifrst = "H" : Normal state 2) ifrst = "L" : Reset state	
4	icsy	I	select composite signal/horizontal signal 1) icomps = "H" : icsy is composite sync signal (high active) 2) icomps = "L" : icsy is horizontal sync signal(low active)	
5	icomps	I	select composite sync mode/separate sync mode 1) icomps = "H" : composite sync mode 2) icomps = "L" : separate sync mode	Note1)
6	iclkc	I	select PLL mode/external clock mode 1) iclkc = "H" : PLL mode 2) iclkc = "L" : external clock mode	Note1)
7	iomclk	I/O	input clock signal (external clock mode) 1) iclkc = "H" : This signal will be ground 2) iclkc = "L" : This signal will be external input ternimal	
8	opsi	O	control decorder chip pin	Fig.9
9	opsc	O	control Dimming for inverter	Fig.10
10	opols	O	polarity alternating signal for video	
11	opolc	O	polarity alternating signal for Vcom	
12	oblk	O	blanking control pin 1) oblk ="H" : blanking display (black) 2) oblk ="L" : normal display	Fig.8
13	onpo	O	auto detect pin for NTSC/PAL 1) onpo ="H" : NTSC 2) onpo ='L" : PAL	Note2)
14	iohsy	I/O	input/output horizontal sync. signal (low active) 1) iclkc = "H" : This signal outputs horizontal sync. signal 2) iclkc = "L" : This signal will be external horizontal sync. Input.	
15	iovsy	I/O	input/output vertical sync. signal (low active) 1) iclkc = "H" : This signal outputs vertical sync. signal 2) iclkc = "L" : This signal will be external vertical sync. Input.	
16	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
17 18 19	imode1 imode2 imode3	I I I	select display mode (1440, 1200 mode only)	Note4)

imode1	imode2	imode3	Description
L	L	L	Full mode
H	L	L	Normal center mode
L	H	L	Normal wide mode
H	H	L	Zoom1 mode
L	L	H	Zoom2 mode
H	L	H	Normal left mode
L	H	H	Normal right mode
H	H	H	Zoom3 mode

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>20
21</td><td>ivpos1
ivpos2</td><td>I
I</td><td>select vertical start line
<table>
<tr><th>ivpos2</th><th>ivpos1</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>L</td><td>L</td><td>20</td><td>26</td></tr>
<tr><td>L</td><td>H</td><td>21</td><td>28</td></tr>
<tr><td>H</td><td>L</td><td>22</td><td>30</td></tr>
<tr><td>H</td><td>H</td><td>23</td><td>31</td></tr>
</table></td><td></td></tr>
<tr><td>22</td><td>VSS</td><td>-</td><td>Ground</td><td></td></tr>
<tr><td>23
24</td><td>ihpos1
ihpos2</td><td>I
I</td><td>select horizontal start point (iclkc ="L" only, ext clock mode)
<table>
<tr><th>ihpos2</th><th>ihpos1</th><th>1440</th><th>1200</th><th>960</th></tr>
<tr><td>L</td><td>L</td><td>100</td><td>85</td><td>67</td></tr>
<tr><td>L</td><td>H</td><td>101</td><td>86</td><td>68</td></tr>
<tr><td>H</td><td>L</td><td>102</td><td>87</td><td>69</td></tr>
<tr><td>H</td><td>H</td><td>103</td><td>88</td><td>70</td></tr>
</table></td><td>Note5)</td></tr>
<tr><td>25</td><td>iarea_sel</td><td>I</td><td>select display range
1) iarea_sel = "H" : The display range is 50.01us (NTSC)
2) iarea_sel = "L" : The display range is 48.00us (NTSC)</td><td>Note1)</td></tr>
<tr><td>26</td><td>iimode</td><td>I</td><td>select simultaneous mode/sequential mode
1) iimode ="H" : simultaneous mode (stripe arrangement)
2) iimode ="L" : sequential mode (delta arrangement)</td><td>Note1)</td></tr>
<tr><td>27</td><td>icpo_sel</td><td>I</td><td>select horizontal position adjust (iclkc = "H" only)
1) icpo_sel = "H" : hor. Position adjustment is normal
2) icpo_sel = "L" : hor.position adjustment is more wide</td><td>Note1)</td></tr>
<tr><td>28</td><td>icph_sel</td><td>I</td><td>select ocph1,2,3 phase (delta arrangement module only)
1) icph_sel = "H" : PVI's arrangement
2) icph_sel = "L" : another company's arrangement</td><td>Note1)
Note6)</td></tr>
<tr><td>29</td><td>iodd_sel</td><td>I</td><td>select falling edge of iovsy's position (NTSC, composite sync onl
1) iodd_sel = "H" : iovsy's phase difference is 1.5H (even field)
2) iodd_sel = "L" : iovsy's phase difference is 0.5H (even field)</td><td>Note1)</td></tr>
<tr><td>30</td><td>LVDD</td><td>-</td><td>low voltage power (3.3V only)</td><td></td></tr>
<tr><td>31
32
33</td><td>ires3
ires2
ires1</td><td>I
I
I</td><td>select resolution mode
<table>
<tr><th>ires1</th><th>ires2</th><th>ires3</th><th>resolution mode</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>1200 * 234</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>-</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>240 * 234</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>480 * 234</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>960 * 234</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>720 * 234</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>1440 * 234</td></tr>
</table></td><td></td></tr>
<tr><td>34</td><td>itest</td><td>I</td><td>select test mode
1) itest = "H" : normal mode
2) itest = "L" : test mode</td><td>Note1)</td></tr>
</table>

No.	Symbol	I/O	Description	Remark
35	itst1	I	select AC/DC test 1) itst1 = "H" : AC/DC test mode 2) itst1 = "L" : normal mode	
36 37 38	ooe3 ooe2 ooe1	O O O	output enable control signal for gate driver ooe1,2,3 ="H" : gate output => Vee 1) ooe1 controls 1 4 7 10 --- 238 lines 2) ooe2 controls 2 5 8 11 --- 239 lines 3) ooe3 controls 3 6 9 12 --- 240 lines	note7)
39	VSS	-	Ground	
40	ostv2	O	gate driver start pulse 1) iund = "H" : ostv2 is in high impedance state 2) iund = "L" : ostv2 is output pin of start pulse	note7)
41	ostv1	O	gate driver start pulse 1) iund = "H" : ostv1 is output pin of start pulse 2) iund = "L" : ostv1 is in high impedance state	note7)
42	ocpv	O	gate driver shift clock	
43	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
44	iosci	I	input for clock oscillator circuit	
45	oosco	O	output for clock oscillator circuit	
46	VSS	-	Ground	
47	opda	O	output for phase comparative signal for PLL circuit	
48	osrst	O	reset source driver IC (active high)	
49	ocph1	O	source driver shift clock #1	
50	ocph2	O	source driver shift clock #2 1) iimode = "H" : ochp2 is always high signal (stripe arrangement) 2) iimode = "L" : ocph2 is shift clock (delta arrangement)	
51	ocph3	O	source driver shift clock #3 1) iimode = "H" : ochp3 is always low signal (stripe arrangement) 2) iimode = "L" : ocph3 is shift clock (delta arrangement)	
52	osth1	O	source driver start pulse 1) ilnr = "H" : osth1 is output pin of start pulse 2) ilnr = "L" : osth1 is in high impedance state	Note8)
53	osth2	O	source driver start pulse 1) ilnr = "H" : osth2 is in high impedance state 2) ilnr = "L" : osth2 is output pin of start pulse	Note8)
54	oq2h	O	pin of RGB output data order on no rotation mode 1) iimode ="H" : no use (low) 2) iimode ="L" : use (delta arrangement)	
55	LVDD	-	low voltage power (3.3V only)	
56	ooeh	O	output enable control signal for source driver 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	
57	ocpo	O	output for horizontal position adjustment	
58	VSS	-	Ground	
59	icpi	I	input for horizontal position adjustment	

No.	Symbol	I/O	Description	Remark
60	iq2h_sel	I	select oq2h phase (delta arrangement only) 1) iq2h_sel = "H" : PVI's arrangement 2) iq2h_sel = "L" : another company's arrangement	Note1) note6)
61	ioeh_sel	I	select perioty of ooeh 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	Note1)
62	ilnr	I	select left/right direction 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1) Note8)
63	iund	I	select up/down direction 1) iund = "H" : normal scan 2) iund = "L" : reverse scan	Note1) Note7)
64	innp	I	select NTSC/PAL 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1)

Note1) Those pins are Normally pull-up
Note2) If use auto detection, this pin must connect innp
Note3) If you want to use 5V's I/O signal, It must connect 5V's Voltage,
otherwise, if you want to use 3.3V's I/O signal, it must connect 3.3V's voltage
Note4) Those pins are Normally pull-down
Note5) This count means No.of input clock from the falling edge of iohsy
Note6) If you use another company's TFT LCD module, please contact PVI.
Note7) iund controls up/down direction
1) iund = "H" : ostv1 → G1(ooe1) → G2(ooe2) → G3(ooe3) → G4(ooe1) → G5(ooe1) → --- → G238(ooe1) → G239(ooe2) → G240(ooe3) → ostv2
2) iund = "L" : ostv1 ← G1(ooe1) ← G2(ooe2) ← G3(ooe3) ← G4(ooe1) ← G5(ooe1) ← --- ← G238(ooe1) ← G239(ooe2) ← G240(ooe3) ← ostv2
Note8) ilnr controls left/right direction
1) ilnr = "H" : osth1 → ----- → osth2
2) ilnr = "L" : osth1 ← ------ ← osth2

6.Service Tools and Equipment

6.1Service Tools and Equipment Table

Application	Name
General	DVD Testing Disc
	General Tools（screwdriver etc.）
Confirm	CD Testing Disc
	VCD Testing Disc
Adjust	Oscillograph
	Probes
	AV Cables
	TV Monitor
Grounding for electrostatic breakdown	Searing-iron
	Antistatic wrist strap
	Conductive material（steel sheet）

6.2 Storing and Handling Test Discs

It is important for a DVD testing disc keeping its surface precise. Please care for storing and using it.

1. Do not place the disc on worktable directly after using.
2. Do not store discs in places subject to direct sunlight or near heat sources.

3. Do not place the disc on a glass surface. It may damage the disc. If this happened, please use a new testing disc adjust DVD player precision.

6.3 Notes

PLEASE READ ALL NOTES GIVEN IN THIS MANUAL.

■ **Locate**

- Place the unit on a firm, flat surface.
- Do not place in a high temperature (upwards of 35℃) or high wet (upwards of 90 percent) area.
- Do not place in an area with a lot of dust.
- Keep away from direct sunlight &domestic heating equipment.

■ **Do not fall any objects into the unit.**

- Care should be taken so that liquids are not spilled into the unit openings. Such situations could result in fire or electrical shock.
- Keep the DVD video player away from any magnetic articles such as speaker etc.

■ **Superposition**

- Please place the DVD player horizontally. Do not place a heavy object (amplifier, receiver) on it. The object may fall, causing serious

personal injury or death.

This unit should be situated away from heat source, such as amplifiers, radiators, stoves or any other units producing heat.

Condensation

Lens could be moistening in these cases.

Turn on heater shortly,

In a very wet room,

Move the player from a cold environment to a heat environment quickly.

Being moisture inside the play could operate normally. Please turn on power and wait about an hour for drying the moisture.